REMARKS/ARGUMENTS

Applicant thanks the Examiner for the thorough consideration given the present application. Claims 1-4 and 6 are pending in the present application. Claims 1, 3 and 6 have been amended. Claim 5 has been cancelled. Claims 1 and 6 are independent claims. The Examiner is respectfully requested to reconsider and withdraw the outstanding rejections in view of the amendments and remarks as set forth hereinbelow.

Claim for Priority

It is gratefully acknowledged that the Examiner has recognized the Applicant's claim for foreign priority. In view of the fact that the Applicant's claim for foreign priority has been perfected, no additional action is required from the Applicant at this time.

Drawings

It is gratefully acknowledged that the Examiner has accepted the Formal Drawings filed on May 11, 2001 for examination purposes. It is respectfully submitted that the Formal Drawings comply with the requirements of the USPTO. If the Official Draftsperson has any objections to the Formal Drawings, he is respectfully requested to contact the

undersigned as soon as possible so that the appropriate action may be taken.

Rejection Under 35 U.S.C. § 112

Claim 5 stands rejected under 35 USC § 112, second paragraph, as being indefinite. In particular, the Examiner rejects this claim because "the period of the clock pluses" in line 2 contains insufficient antecedent basis. Applicant respectfully submits that claim 5 has been cancelled above and, thus, this rejection has been rendered moot.

Synopsis of the Present Invention

Before turning to the rejections a brief synopsis of the invention is presented.

In accordance with the present invention, a device for high-speed access, a device low-speed access and a control circuit for controlling data transfers to these devices are connected by a common bus in such a manner that gives priority to data transfers to the device for high-speed access. A switch circuit is provided between the device for high-speed access and the device for low-speed access to perform the function of turning on and off this bus connection. The switch circuit is controlled so as to turn off the bus connection when data is transferred to the device for

high-speed access, and to turn on the bus connection when data is transferred to the device for low-speed access.

When the switch circuit turns off the common bus connection, the device for low-speed access is disconnected from the common bus while data is transferred to the device for high-speed access. Since the length of the common bus is essentially shortened in this situation, the present invention makes stable operation possible for an integrated circuit operating at high speed.

In particular, common clock pulses are sent to each of the devices for high-speed and low-speed access, and to the switch control circuit. Both the high-speed access device and the low-speed access device operate in synchronization with these common clock pulses, the period of which varies depending upon the access speed of the particular device to be accessed. See the specification at page 7: lines 23-28, page 10: lines 13-25, and Fig. 3. Thus, only one clock pulse generating circuit is used to operate these devices based on the access speed of the device to be accessed.

Rejection Under 35 U.S.C. § 103

Claims 1 and 6 stand rejected under 35 USC § 103(a) as being unpatentable over Japanese Patent Document No. JP 2000020459 A to Nakajima et al. (hereinafter Nakajima) in view

of U.S. Patent No. 5,481,679 to Higaki et al. (hereinafter Higaki). This rejection, insofar as it pertains to the presently pending claims, is respectfully traversed.

As amended, independent claim 1 now recites that "the device for high-speed access, the device for low-speed access and the switch control circuit each operates in synchronization with common clock pulses, the common clock pulses having a period that varies based on the access speed of the device to be accessed." Applicant respectfully submits that this feature is neither taught nor suggested by the cited prior art.

Nakajima

In Nakajima, although the rapid access field 2 is directly linked with CPU 1 through a data bus 4, the other usual access fields 3 are connected to CPU 1 through a bus switch 5. (The Examiner interprets element 3b of usual access field 3 to read on the claimed device for low-speed access -- see page 6 of the Office Action.) The bus switch 5 controls the electrical connection/disconnection between the usual access field 3 and CPU 1 based on the operation of the bus control section 6. Specifically, at a time of connection, a low impedance exists between the bus switch 5 and the I/O 3a. At a time of disconnection, there is a high impedance between the bus switch 5

and I/O 3a that causes the relationship and operation between the access field 3, and the CPU 1 and rapid access field 2.

Higaki

Higaki is relied upon by the Examiner merely to disclose an electronic instrument implemented in an integrated circuit.

Yasukawa

Yasukawa discloses a data transfer apparatus, which includes circuit A (2) and circuit B (3), which are connected to each other through line 10 and operate independently of each other at different clock frequencies. Specifically, circuit A operates according to a clock signal Clock_A, while circuit B operates according to a clock signal Clock_B, which has a lower clock frequency of Clock_A. See Yasukawa at column 4: lines 32-39.

Claims 1 and 6 Not Obvious In View of Cited Prior Art

Accordingly, Nakajima, Higaki, and Yasukawa, either taken alone or in combination with one another, do not teach or suggest that each of the devices for high-speed and low-speed access and the switch control circuit operates in synchronization with common clock pulses whose period varies based on the access speed of the device to be accessed, as required by independent claim 1.

In the Office Action, the Examiner asserts that Yasukawa discloses clock pulses whose period varies independent upon the access speed of the device to be accessed, citing Yasukawa's disclosure that the period of signal Clock_A differs from Clock_B (see pages 7-8 of the Office Action). However, Applicant respectfully submits that Yasukawa fails to disclose that Clock_A and Clock_B correspond to common clock pulses sent to devices for high-speed access and low-speed access. Rather, in Yasukawa, Clock_A and Clock_B represents the frequencies of different clock signals sent to circuits A and B. Accordingly, Yasukawa requires at least two clock signal generating circuits.

Conversely, claim 1 requires that the devices for high-speed access and low-speed access, in addition to the switch control circuit, each operates in synchronization with common -- not different -- clock pulses.

Thus, Applicant respectfully submits that independent claim 1 is allowable at least for the reasons set forth above. Also, Applicant submits that independent claim 6 recites features similar to those identified above with respect to independent claim 1 and is therefore allowable at least for similar reasons. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Claim 2 Not Obvious

In the Office Action, the Examiner rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Nakajima as applied to claims 1 and 6, and further in view of U.S. Patent No. 6,061,754 to Cepulis et al (hereinafter Cepulis). Applicant respectfully submits that claim 2 is dependent upon independent claim 1, and therefore incorporates the features recited in claim 1. Accordingly, Applicant presumes the Examiner intended to reject claim 2 as being obvious over Nakajima and Higaki, as applied to claims 1 and 6, and further in view of Cepulis.

Applicant respectfully submits that Cepulis fails to remedy the deficiencies of Nakajima and Higaki set forth above in connection with independent claim 1. Accordingly, Applicant respectfully submits that claim 2 is allowable at least by virtue of it dependency on independent claim 1.

Claims 3 and 4 Not Obvious

In the Office Action, the Examiner rejected claims 3-5 under 35 U.S.C. § 103(a) as being unpatentable over Nakajima, as applied to claims 1 and 6, and further in view of Yasukawa. Since originally filed claims 3-5 were dependent on independent claim 1, and therefore incorporated the elements recited in claim 1, Applicant presumes the Examiner intended to reject claims 3-5 as

being obvious over Nakajima and Higaki, as applied to claims 1 and 6, and further in view of Yasukawa.

Initially, Applicant respectfully submits that claim 5 has been cancelled. Accordingly, this rejection as applied to claim 5 is rendered moot.

Applicant further submits that the combination of Nakajima, Higaki and Yasukawa fails to provide a teaching or suggestion of each feature recited in independent claim 1 at least for the reasons set forth above. Accordingly, Applicant respectfully submits that claims 3 and 4 are allowable at least by virtue of their dependency on independent claim 1.

Conclusion

Since the remaining patents cited by the Examiner have not been utilized to reject the claims, but to merely show the state of the art, now comment need be made with respect thereto.

In view of the above amendments and remarks, Applicant respectfully submits that all of the pending claims are now in condition for allowance. This, the Examiner is respectfully requested to reconsider and withdrawal the outstanding rejections.

Should the Examiner believe that any outstanding matters remain in the present application, the Examiner is respectfully

requested to contact Jason W. Rhodes (Reg. No. 47,305) at the telephone number of the undersigned in order to conduct an interview to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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